Comparator Circuits Having Non-Complementary Input Structures
Gabara 80
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FIG. 1
PRIOR ART
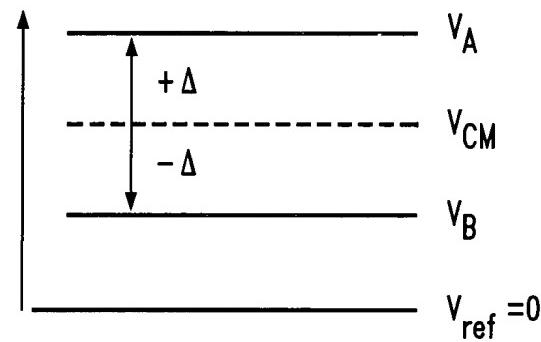
FIG. 2
PRIOR ART

(A)
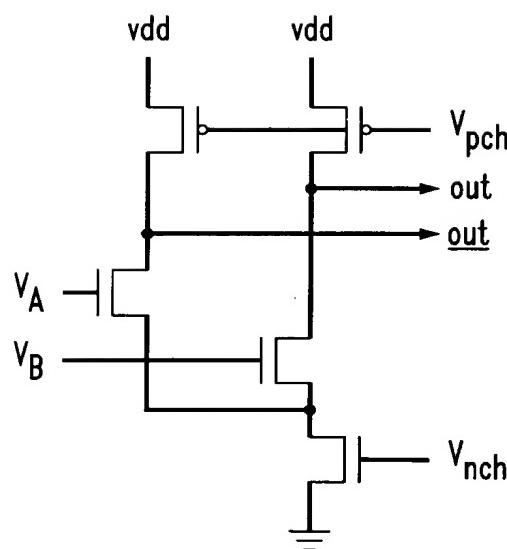
(B)
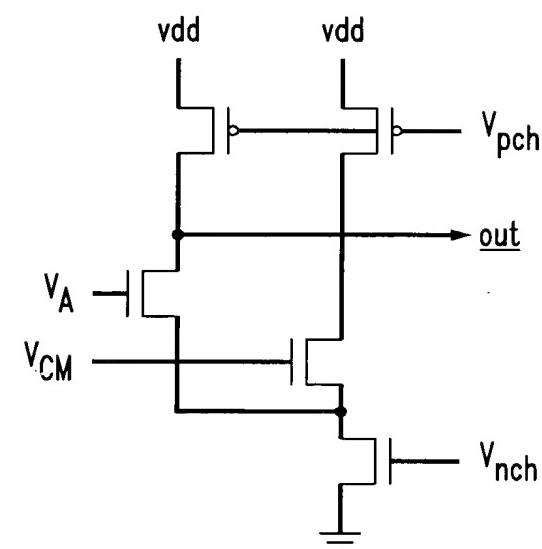
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FIG. 3
PRIOR ART
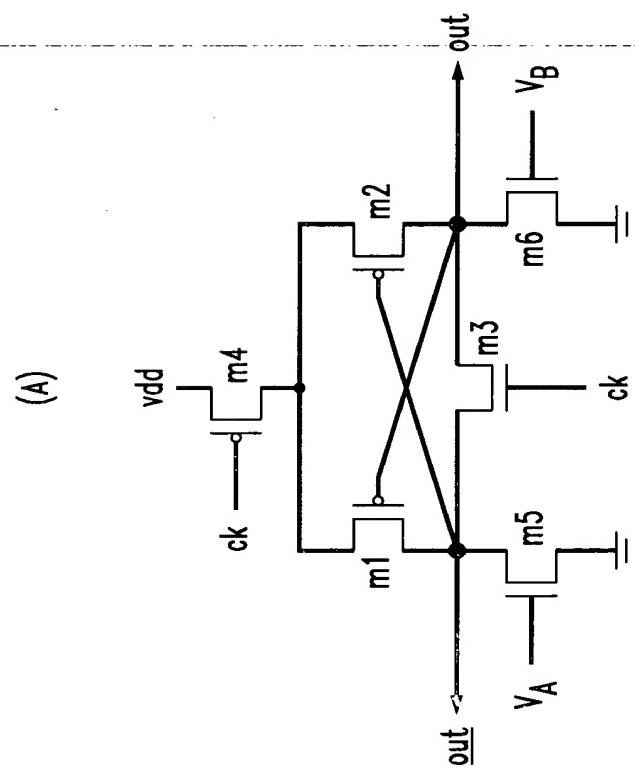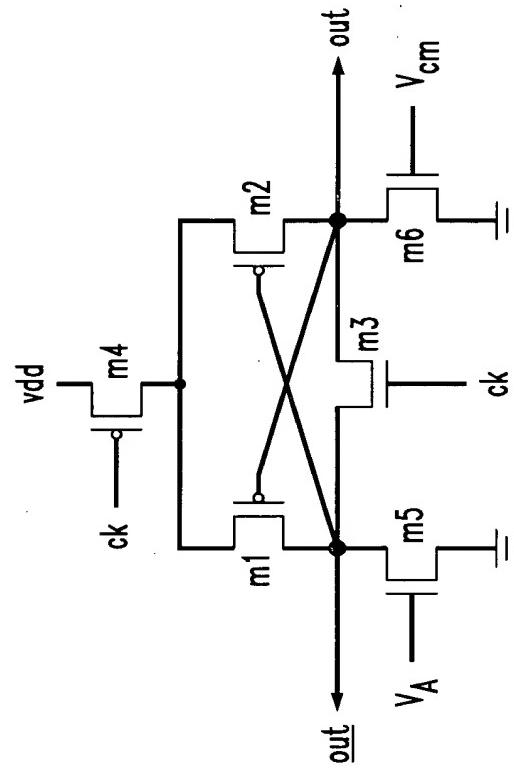
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FIG. 4
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FIG. 5
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FIG. 6

PRIOR ART

(A)

(B)

(C)

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FIG. 7

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FIG. 8

FIG. 9

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FIG. 10A

FIG. 10B

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FIG. 10C

FIG. 10D

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FIG. 11

vdd

ck ─┤ m9

m1   m2

outn ←   → out

m3   m4

in₁ → $R_1 = F(in_1)$ $R_2 = F(in_2)$ ← in₂

FIG. 12

TIME

ck   SETUP TIME

in₁,₂

out/outn   DTA ATD DIGITAL

ANALOG EVALUATION (1nsec)

DIGITAL INPUT   DIGITAL OUTPUT

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FIG. 13

ck_{1-2}

RAM CELL

outn ←

out →

$in_1 \rightarrow$ | $R_1 = F(in_1)$ | | $R_2 = F(in_2)$ | $\leftarrow in_2$

FIG. 14

$in_1 \rightarrow$ | $R_1 = F(in_1)$ | | $R_2 = F(in_2)$ | $\leftarrow in_2$

WIDTH =   WIDTH =

2^{n-1} 2^2 2^1 2^0 2^0 2^1 2^2 2^{n-1}

a_{n-1} —| | |— b_{n-1}

a_2 b_2
a_1 b_1
a_0 b_0

FIG. 15

WIDTH =

2^{n-1} 2^2 2^1 2^0

a_{n-1} —| | |— offset

a_2
a_1
a_0

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FIG. 16

TIME

Out0-7   "1"   "0"   Outn0-7

2^7 2^1 2^0 2^{-1} 2^{-1} 2^0 2^1 2^7

a_7 $\cdots$ b_7

a_1 b_1

a_0 b_0

RAM CELL

ck_{1-2}

Out8-15   Outn8-15

2^7 2^1 2^0 2^{-1} 2^{-1} 2^0 2^1 2^7

a_{15} $\cdots$ b_{15}

a_9 mon   moff b_9

a_8 b_8

mn1

RAM CELL

ck_{2-3}

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FIG. 17

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FIG. 17 (CONT'D)

ck^1

ck^2

ck^3

TIME

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FIG. 18

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FIG. 18 (CONT'D)

ck^1

ck^2

ck^3

ck^1

ck^2

ck^3

TIME

FIG. 19

WIDTH = 2^0 2^0 2^0 2^0

RAM CELL

ck_{1-2}

2^0 2^0 2^0 2^0

DIGITAL
INPUT = a   b   c   d

out   out

w   x   y   z

FIG. 20

WIDTH = 2^0 2^0 2^0 2^0

RAM CELL

ck_{1-2}

2^0 2^0 2^0 2^0

ANALOG
INPUT = a   a   b   b

out   out

c   c   d   d

FIG. 21

in	out2	out1
≤1000	1	1
>1001	1	0
<1100	1	0
≥1100	0	0

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FIG. 22

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FIG. 23
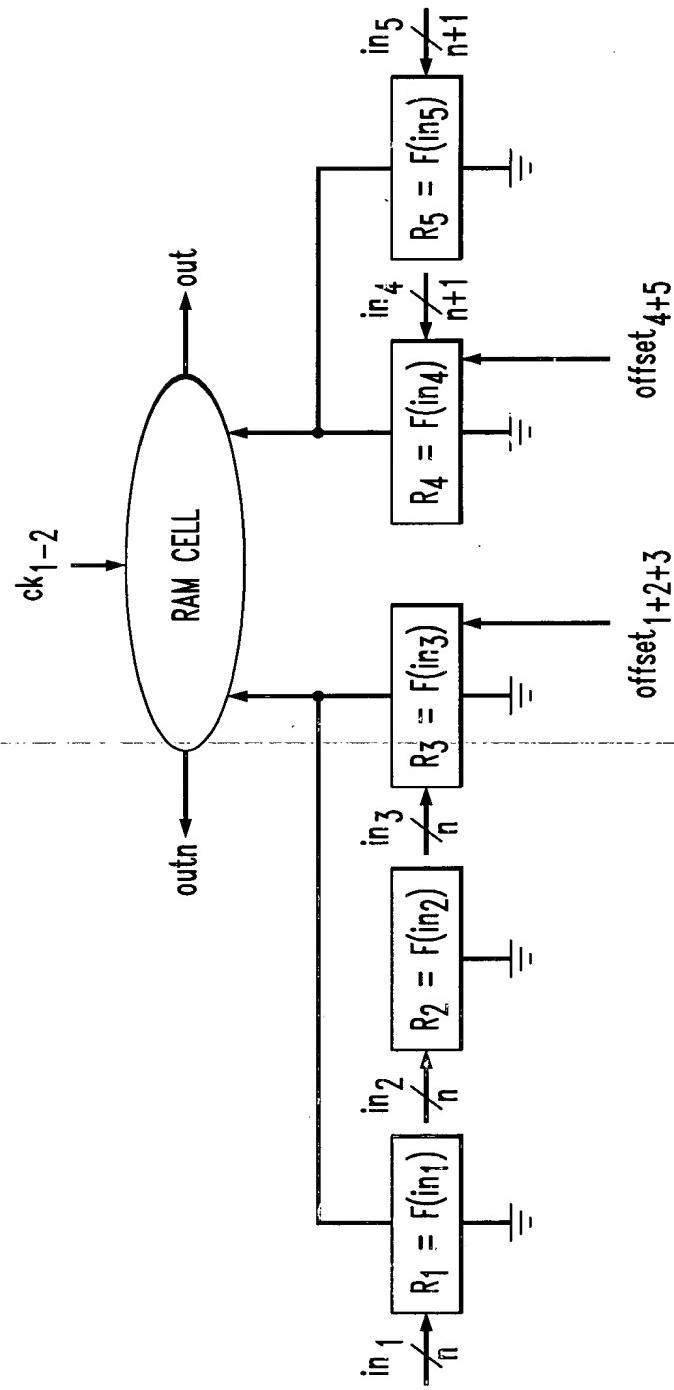
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FIG. 24A

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FIG. 24B

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FIG. 25

out

ck_{1-2}

RAM CELL

2^0 = WIDTH

2^1

2^{n-2}

2^{n-1}

a_0

a_1

a_{n-1}

a_n

132

0 | 0 | ... | 0 | 1

2^{-1}

OFFSET = vdd

OFFSET HELPS
LEFT SIDE WIN
IN A TIE

CARRY OUT BIT

FSM

130

outn

$R_2 = F(in_2)$

in_2 / n

$R_1 = F(in_1)$

in_1 / n

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FIG. 26

```
/* initialize */
n=8 ;
a[n] = 1;
for (k=1; k<n; k++)
   a[k]=0;

for (i=0; i<n; ++i) /* i=clock tick*/
  if (out = 0)
     a[n-i-1] = 1;
  else {
     a[n-i] = 0;
        if (i < n - 1)
           a[n-i-1] = 1;
  }
/* addition result is in array a[n] */
```

FIG. 27

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FIG. 28
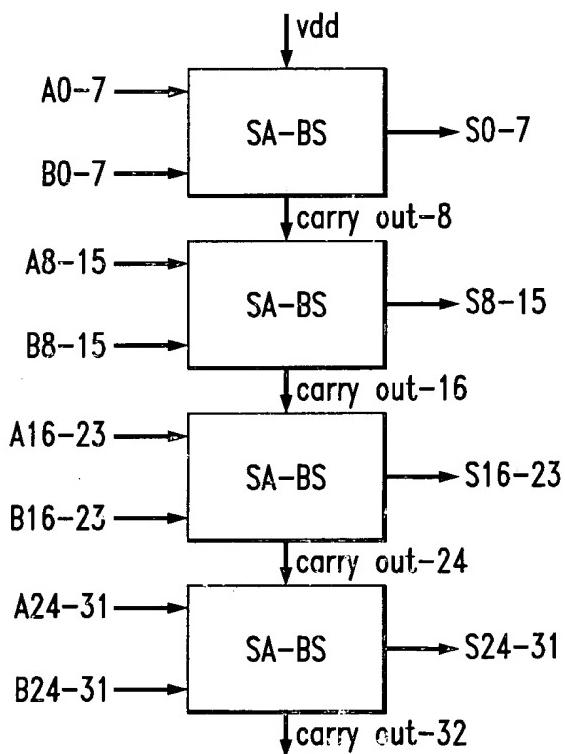
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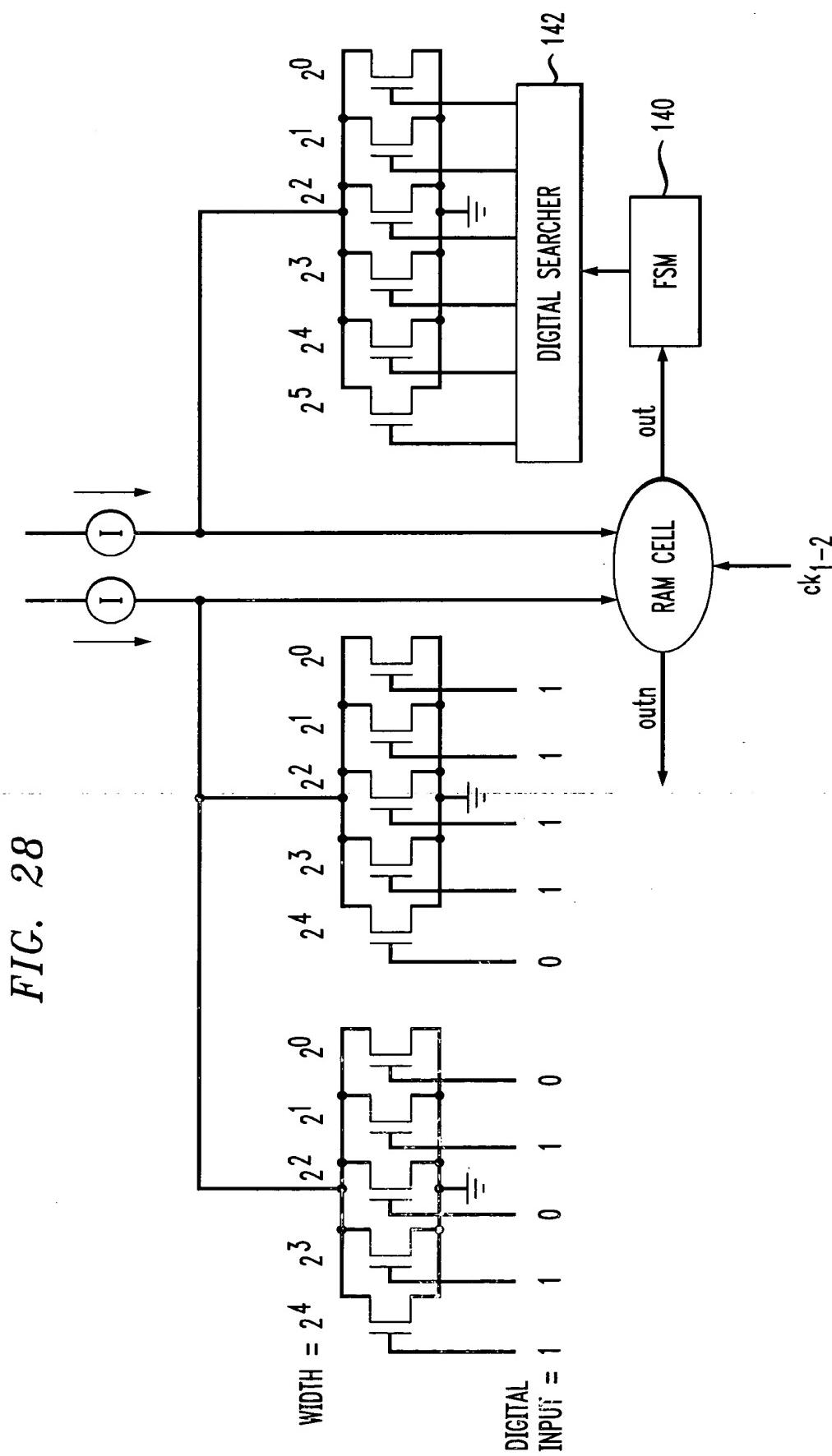
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FIG. 29

PRIOR ART

FIG. 30

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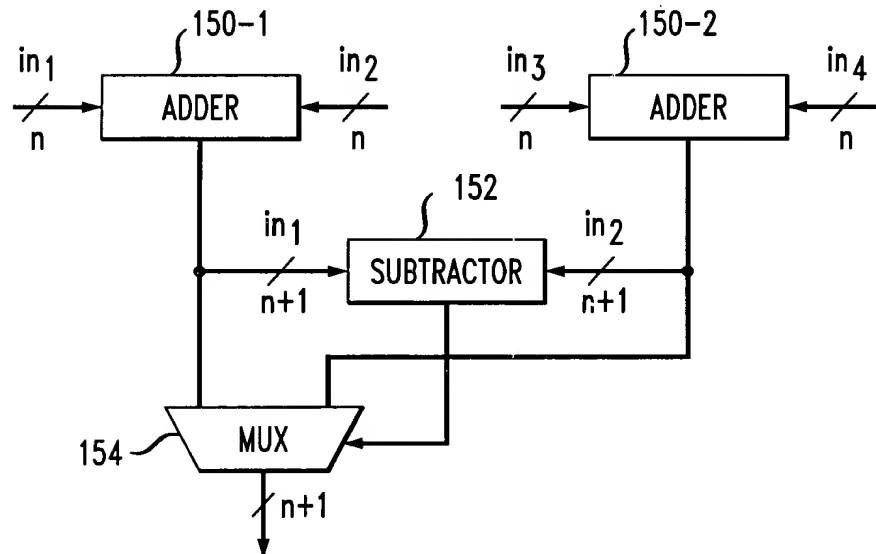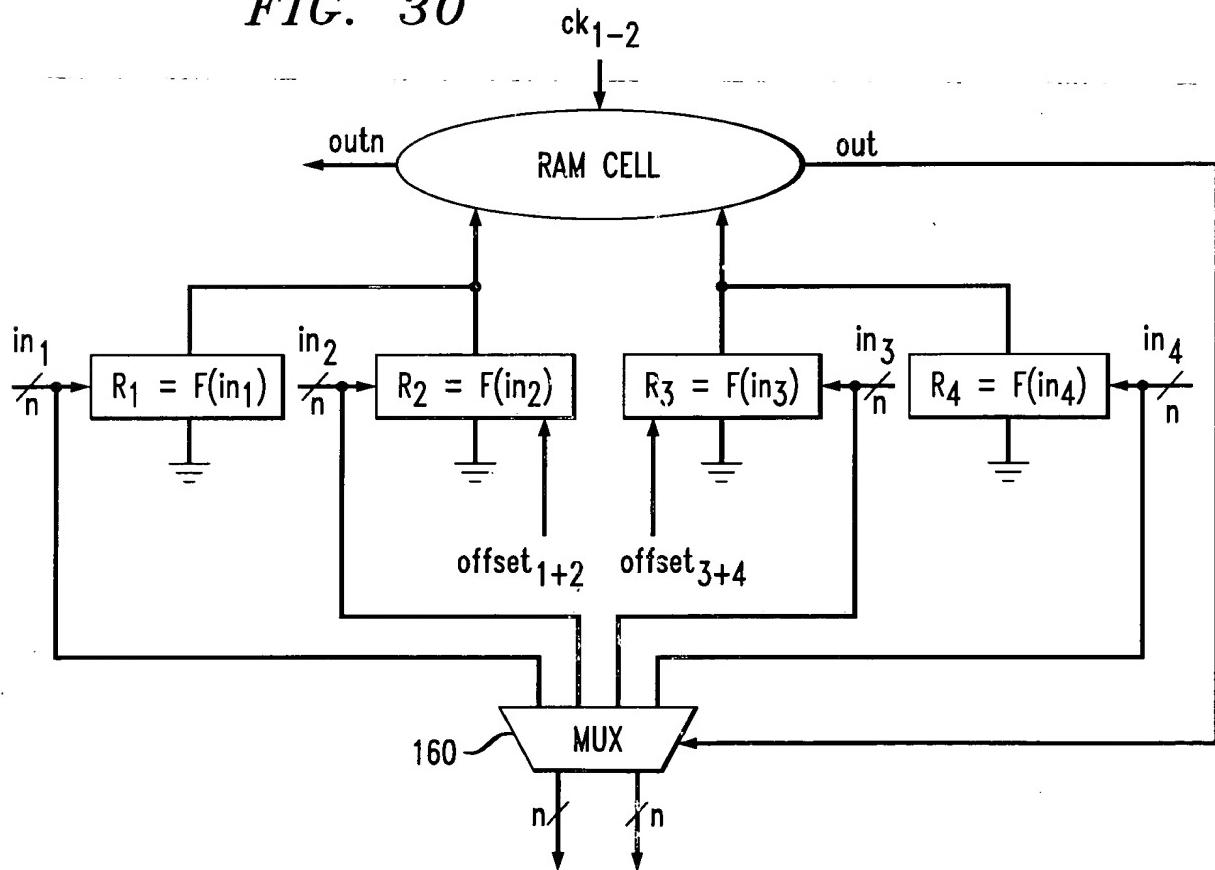
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FIG. 31
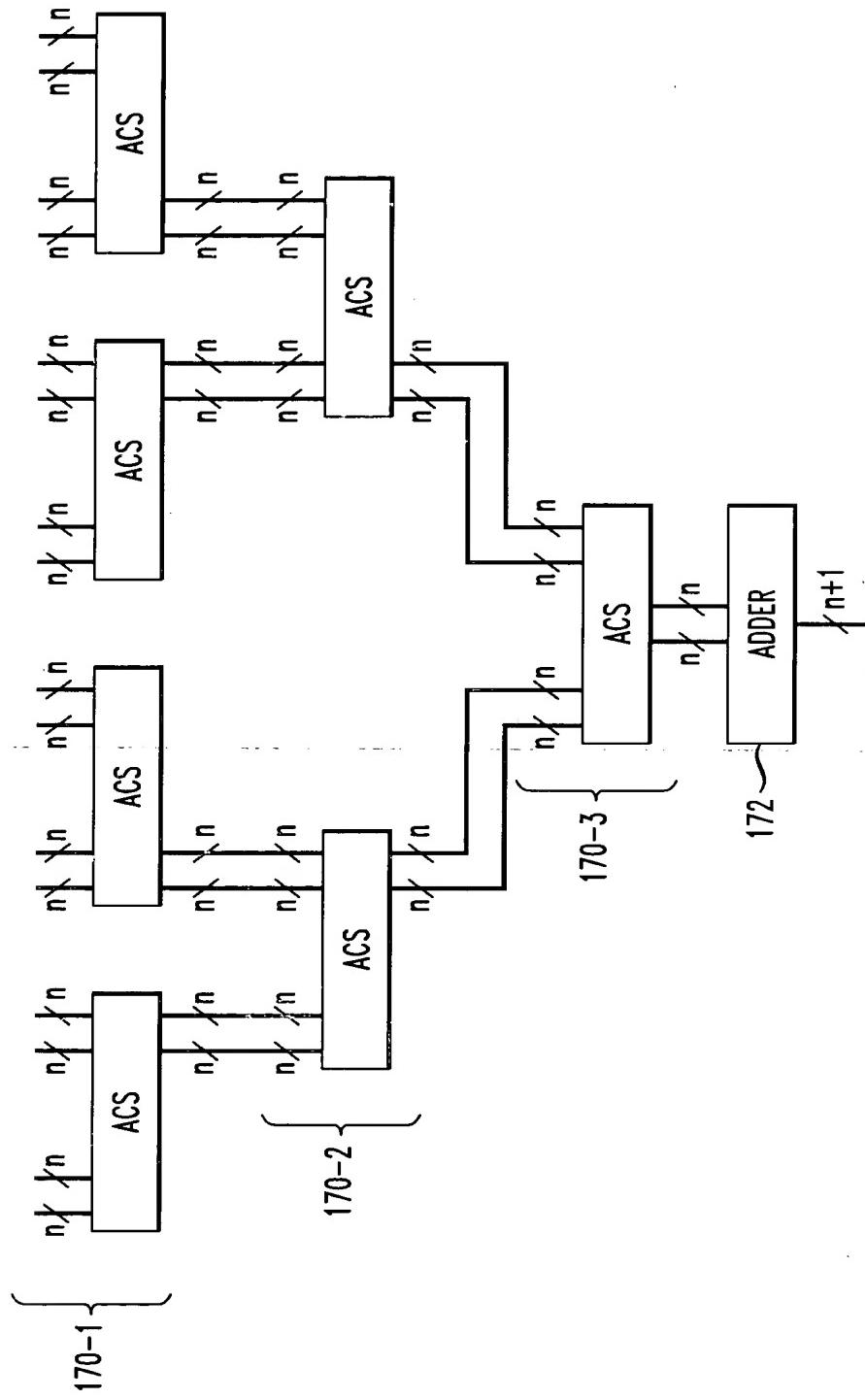
FIG. 32

	POWER (μW)		TRANSISTOR COUNT		DELAY (pSEC)	
	ADD COMPARE	SELECT	ADD COMPARE	SELECT	ADD COMPARE	SELECT
CONVENTIONAL	2000	200	5215	58	1120	200
SEESAW	100	300	55	108	516	173
GAIN FACTOR	X20	X0.66	X95	X0.54	X2.17	X1.15

FIG. 33

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FIG. 34

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FIG. 35

FIG. 36

vdd ↓I

in_2 → $R_2 = F(in_2)$ 180 $R_1 = F(in_1)$ ← in_1

outn → DIFF AMP ← out

in_1 → $R_1 = F(in_1)$ $R_2 = F(in_2)$ ← in_2